REMARKS

Claims 1-36 are pending. In the Office Action dated December 22, 2006, the Examiner rejected claims 1-36 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,587,912 to Leddige et al.

The disclosed embodiments of the invention will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

As the operating speed of processor-based systems continues to increase, it has become more important to precisely control the timing at which signals are transferred between different components of such systems. For example, processor-based systems using memory modules containing a memory hub coupled to a plurality of memory devices operate at a very high rate of speed. In such systems it can be difficult to coordinate the coupling of read data from the memory devices to the memory hub and from the memory hub to other components in the processor-based system.

In one embodiment, the above problem is addressed by the disclosed memory hub, which includes a read synchronization module that is coupled to the memory devices. The read synchronization module compares the timing between when read data are coupled from the memory devices, generally responsive to a read data strobe signal, and the timing when the read data are coupled from the memory hub, which is generally in synchronism with a core clock signal. Based on this comparison, the disclosed read synchronization module generates an adjust signal. The adjust signal is applied to a memory sequencer, which couples memory requests to the memory devices responsive to received memory requests. The memory sequencer uses the adjust signal to adjust the timing at which read memory requests are coupled to the memory devices. As a result, the memory sequencer can control the timing at which the read data are coupled from the memory devices to the memory hub. In this way, the timing at which the read data and read data strobe signal are coupled from the memory device to the memory hub can be synchronized to a core clock signal that is used to clock the read data from the memory hub to

another component in a processor-based system, such as a memory hub controller. Also, the optimum bandwidth through the memory hub can be achieved because the read data are coupled from the memory hub to a memory access device as soon as the memory hub receives the read data from a memory device.

The Examiner has cited the Leddige *et al* reference. The Leddige reference is directed toward a memory system that implements the use of multiple memory buses on a memory module to increase the number of memory devices that can be used on each memory module. In Figure 3, each memory module 210a, 211a, and 212a includes a memory repeater hub 320, 330, and 340, respectively. In memory module 210a, a first memory bus 300 is coupled in series to a second memory bus 321 and a third memory bus 322, which are coupled to each other in parallel. The coupling of additional memory buses to the first memory bus 300 via the memory repeater hub 320 allows for more memory devices to be added to the memory system.

The Examiner contends that the memory repeater hub performs the function of the read synchronization module and memory sequencer in the present application. In particular, the Examiner contends that clock buffer 716, address interface circuit 718, control interface circuit 719, data I/O circuit 722, and control logic 702, shown in Figure 7, disclose a read synchronization module that is operable to compare timing between when read data are coupled from the memory devices and the timing when read data are coupled from the memory hub. This is not correct. While the clock generator 710 may operate clock signal 730 at a different frequency than clock signal 724, none of the components disclosed in the Leddige reference are capable of comparing the timing of the clock signals and generating an adjust signal corresponding to the compared timing. Rather, the Leddige reference merely states that the clock signal frequencies 724 and 730 may be either the same or different from one another. *Leddige Specification*, column 9, lines 17-27.

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. Independent claim 1 recites, in part, "a read synchronization module....operable to compare timing between coupling read data from the memory devices and coupling read data from the memory hub and to generate an adjust signal corresponding to the compared timing." The Leddige reference does not disclose or fairly suggest this limitation. Rather, the Leddige reference merely discloses that the clock

signals may be different from one another, but does not disclose the capability of comparing the timing and generating an adjust signal corresponding to the compared timing. Therefore, claim 1 is allowable over the Leddige reference.

Independent claim 13 is directed to the memory hub that is included in the memory module of claim 1 and is, therefore, allowable over the Leddige reference for at least the same reasons that claim 1 is allowable.

The memory module of claim 1 is claimed in the context of a computer system in independent claim 20, and is therefore allowable for at least the same reasons that claim 1 is allowable.

Independent claim 8 recites, in part, "a read synchronization module...operable to compare timing between the read data strobe signals and a core clock signal and to generate an adjust signal corresponding to the compared timing." As stated above, the Leddige reference merely discloses that the clock signals may be different from one another, but does not disclose or fairly suggest the capability of comparing the timing and generating an adjust signal corresponding to the compared timing. Therefore, claim 8 is allowable over the Leddige reference.

Independent claim 27 is directed to a method of reading data form a memory module and recites, in part, "comparing timing between receiving the read data and outputting the read from the memory module and adjusting the timing at which read memory requests are coupled to the memory device interface as a function of the compared timing." Again, the Leddige reference does not disclose or fairly suggest this limitation. The Leddige reference merely discloses that the clock signals may be different from one another, but does not disclose comparing the timing between receiving read data and outputting the read. In addition, because the Leddige reference does not disclose comparing the timing, it also does not disclose adjusting the timing as a function of the compared timing. Therefore, claim 27 is allowable over the Leddige reference.

Independent claim 33 is directed toward a method of coupling read data from a memory device to a buffer and outputting read data from the buffer and recites, in part, "comparing timing between storing the read data in the buffer and outputting the read from the buffer and adjusting the timing at which read memory requests are coupled to the memory device

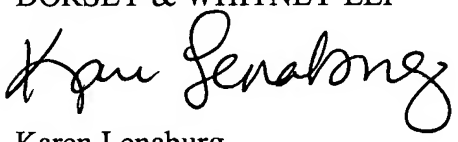
interface as a function of the compared timing." Similar to the statement above, the Leddige reference does not disclose or fairly suggest the above limitation. Although the Leddige reference discloses that clock signals may be different from one another, it does not disclose comparing timing between receiving read data and outputting the read from a memory module. Rather, it merely discloses that the clock signals may be different from one another. Therefore, claim 33 is allowable over the Leddige reference.

Claims depending from the above independent claims are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims.

All of the claims in the application are clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



Karen Lenaburg
Registration No. 58,371
Telephone No. (206) 903-2399

KL:sp

Enclosures:
Postcard
Fee Transmittal Sheet (+copy)

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

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